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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/736,755

12/17/2003

Philippe Antoine

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EXAMINER

PANWALKAR, VINEETA S

ART UNIT

PAPER NUMBER

2611

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

04/17/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/736,755

Applicant(s)

ANTOINE ET AL.

Examiner

Vineeta S. Panwalkar

Art Unit

2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 8-10 is/are rejected.
- 7) ☒ Claim(s) 4-7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 December 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12/17/03</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

- 1a. The drawings are objected to because the numbers used as labels in Figs. 1 and 2 are not descriptive. Although the specification mentions what each of the numbers in Figs. 1 and 2 stands for, it is suggested that descriptive labels be used in the drawings to further clarify the invention.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

- 1b. The abstract of the disclosure is objected. "Figure 1 is attached" in line 20 needs to be deleted because the abstract needs to commence on a separate sheet. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

Art Unit: 2611

U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1,2,8,9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peeters (US 6947372 B2), hereinafter, Peeters, in view of Anne et al. (US 2003/0081741 A1), hereinafter, Anne.

- 2a. Regarding claims 1, 8, 9 and 10, Peeters shows an integrated modem circuit comprising:

- a processor-system and hardware for exchanging signals with another modem circuit (See column 4, lines 18-38. A multi-carrier communication system wherein data are transferred bi-directionally (claimed exchanging of signals) in a time division duplexed way between two transceivers (claimed hardware wherein the modems are claimed integrated and another modem circuits) is shown);
- wherein integrated modem circuit comprises a digital phase locked loop filter (Figs. 3 the phase locked loop PLL1 is interpreted as claimed digital phase locked loop because it comprises between its input terminals and its output terminals a filter (FILTER1));
- characterized in that said integrated modem circuit exchanges signals with another modem circuit at 1 Mb/s or more (FIG. 1 shows a VDSL (Very High Speed Digital Subscriber Line) system, which is capable of speeds greater

than or equal to 1Mbps; see footnote ¹), with said processor-system comprising filter software for embodying said digital phase locked loop filter and with said hardware comprising at least one module for compensating for sample processing (Fig. 3, ROT1 is interpreted as claimed module for compensating for sampling process. The first phase rotor ROT1 in combination with the skip/duplicate unit S/D compensates for the sample rate differences between the transmitter in the line termination VDSL_LT and the receiver in the network termination VDSL_NT.)

(See column 4, lines 20 – 56 and column 5, line 65 – column 6, line 60)

Peeters further states that although no architecture is disclosed, from the functional description of the blocks of the invention, embodiments of these blocks can be manufactured with well-known electronic components. (Column 8, lines 3-12).

Thus, Peeters shows all the limitations claimed (including corresponding method claimed in claim 10), but fails to explicitly mention whether software may be used in implementing the digital PLL and corresponding filter.

However, in the same field of endeavor, Anne shows a modem comprising a digital signal processor (Paragraph [0016]; DSP, interpreted as claimed processor system), wherein the DSP implements a digital phase locked loop

- ¹ References showing that VDSL systems are capable of speed in excess of 1Mbps:
- Halder et al. (US 2003/0112966 A1)
- Zakrzewski et al. (US 2003/0016797 A1)

(claimed software implementation). Regarding claim 9, software implementation using the DSP system is interpreted as claimed program product.

Thus, it would have been obvious to a person of ordinary skill in the art to use software implementation for the DPLL as suggested by Anne in the transceiver system shown by Peeters, because software implementation as suggested by Anne permits robust noise performance and improved noise immunity (Paragraph [0016]).

- 2b. Regarding claim 2, Peeters and Anne show all the limitations claimed (see 2a above)

Peeters further shows the integrated modem circuit according, characterized in that said processor-system comprises sample software for processing samples in dependence of results originating from said phase locked loop filter (Fig. 3, and column 5, line 65 – column 6, line 21. DVCO1 in digital PLL 1 is interpreted as the unit performing claimed processing because it processes the output of the filter).

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peeters in view of Anne as applied to claim 2 above, and further in view of Spruyt et al. (US 6088386), hereinafter, Spruyt.

Art Unit: 2611

- 3a. Regarding claim 3, Peeters and Anne show all the limitations claimed (see 2b above).

Peeters a multi-carrier communication system wherein data are transferred bi-directionally in a time division duplexed way between two transceivers (see column 4, lines 18-38). Thus, a transceiver modems shown in Figs 2 and 3 both include a transmit path and a receive path. Fig. 2 shows the transmission path used in the modems, while Fig. 3 shows the receiving path used.

Thus, Peeters further shows the integrated modem circuit, characterized in that said hardware comprises in a transmission path (Fig. 2), a rotor (Fig. 2, block ROT) and an inverse Fourier transformator (Fig. 2, block IFFT) and in a receiving path (Fig. 3) a Fourier transformator (Fig. 3, block FFT), a rotor (Fig. 3 ROT 1), with at least one of said rotors forming said module (See 2a above).

Peters further discloses that the carriers in the multi-carrier system are modulated with data using discrete multi tone modulation (DMT)(Column 3, lines 50-55 and column 4, lines 19-28).

Thus, Peeters and Andre disclose all the limitations claimed, but fail to explicitly disclose claimed mapper and demapper.

However, in the same field of endeavor, Spruyt shows a modulator/demodulator (MODEM) using DMT equipped with a rotation circuit (TROT) in its transmitting part (TP) and a rotation circuit (RROT) in its receiving part (RP) comprising a mapper (MAP) in it's transmission path TP and a demapper (DMAP) in it's receiving path (RP) (See Fig.1 and column 5, lines 45-67).

Thus, it would have been obvious to a person of ordinary skill in the art to use the mapper and demapper shown by Spruyt in the transceiver system disclosed by Peeters and Anne, because Spruyt's invention reduces complexity of echo cancellation (Column 2, lines 10-16).

Allowable Subject Matter

4. Claims 4-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:
 - Halder et al. (US 2003/0112966 A1) shows that VDSL systems are capable of connection speed in excess of 1Mbps.
 - Zakrzewski et al. (US 2003/0016797 A1) shows how Very-high-data-rate Digital Subscriber Line (VDSL) transceivers are capable of speeds well over 1 Mbps (up to 50 Mbps).
 - Mallory et al. (US 2002/0006136 A1) show software implementation of DPLL.

Art Unit: 2611

- Schelstraete (US 2001/0017900 A1) shows a modem communicating over DSL comprising mapper/demapper, rotors and Fourier and inverse Fourier transformers.

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vineeta S. Panwalkar whose telephone number is 571-272-8561. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



JAY K. PATEL
SUPERVISORY PATENT EXAMINER